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## ABSTRACT OF THE DISCLOSURE

A semiconductor memory device is comprised of a 1 plurality of sense amplifiers. The sense amplifiers are 2 arranged in two amplifier columns. The two amplifier 3 columns are disposed between two cell columns of cell plates. An address circuitry, an ATD circuitry, and a delay circuitry are disposed between an input pin row and 6 the two cell columns. An ATD pulse synthesizer is 7 disposed between the two amplifier columns and spaced a predetermined signal transmission path from the ATD and 10 delay circuitries.